SBX2 — REVISIONS

SCH REV	PCB REV	DATE	BY	DESCRIPTION	SCH REV	DATE	BY	
0.0		00 June 20	wsk	Start of schematic capture based upon unreleased SBX1.				
1	1	00 July 25	wsk	Initial schematic capture complete.				
2	2	00 Aug 22	wsk	Sheet 3: Changed crystal oscillator load caps to 18pF; Added RP15;				
				Sheet 4: Deleted LED1 & R2; Renamed LED2 to LED1; Changed LOCAL_LED(L) to DCE_DCD(L);				
				Sheet 6: Added C20, P9, R13, R14, R15, RP16, RP17, U17; Changed P6 to 2mm header that supports the Systronix DTE / DCE / IrDA Dongle; Deleted R7 & R8; Connected U13 pin 24 to ground;				

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TO DO:

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Title SBX with LCD, KEYPAD, DIG I/O, & SERIAL I/O
REVISIONS

Size	Number		Rev
B			2

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	A	B	C	D	

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Size **B**	Number	Rev **2**
Date Wed Sep 20, 2000	Drawn by B BOYES	
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SERIAL I/O
KPAD_Y5
UART_INT(H)
6

X1
3.6864MHz
U1:A
1 2
74HC04
R3
1M
C1 18pF
C3 18pF

U1:B
3 4
74HC04

U1:D
9 8
74HC04
RST(L)

RST(H)

U14

22	CLK	UARTWR 55
1	RST	UARTRD 63
8	ADDR2	UARTADDR0 77
9	ADDR1	UARTADDR1 85
10	ADDR0	UARTADDR2 92
3	WR	
4	RD	
11	INT0	
13	CS1	LCDEN 53
15	CS0	LCD_WR 35
		LCD_RS 32
12	DAT7	LCDRDOE 64
14	DAT6	
16	DAT5	LCDDATRD 60
17	DAT4	LCDDATWR 52
18	DAT3	MISCSTROBE 61
20	DAT2	
23	DAT1	DOUTWR0 27
25	DAT0	DOUTWR1 29
		DOUTWR2 30
74	LCD_WAIT	DINPRD0 28
56	Y0	DINPRD1 33
68	Y1	DINPRD2 54
90	Y2	BUFDAT7 50
89	Y3	BUFDAT6 49
67	Y4	BUFDAT5 42
87	X0	BUFDAT4 40
91	X1	BUFDAT3 39
95	X2	BUFDAT2 37
97	X3	BUFDAT1 38
		BUFDAT0 36

A2 ADDR2
A1 ADDR1
A0 ADDR0
WR(L)
RD(L)
MINT0(H)
MCS1(L)
MCS0(L)

BA0
BA1
BA2

SERIAL I/O
RST(H)
MCS1(L)
3.6864MHZ
UARTWR(L)
UARTRD(L)
BA[0..2]
BD[0..7]
6

LCD
LCD_EN
LCD_WR(L)
LCD_RS
LCD_DAT_RDOE(L)
LCD_DAT_RD
LCD_DAT_WR
MISCSTROBE
RST(L)
BD[0..7]
4

DIGITAL I/O
DOUT_WR0
DOUT_WR1
DOUT_WR2
DINP_RD0(L)
DINP_RD1(L)
DINP_RD2(L)
RST(L)
BD[0..7]
5

P2 SBX8 EXP MODULE

Pin	Name
1	+12
2	-12
3	GND
4	+5
5	RST
6	MCLK
7	MA2
8	MPST
9	MA1
10	N/C
11	MA0
12	MINT1
13	IOWR
14	MINT0
15	IORD
16	MWAIT
17	GND
18	+5
19	MD7
20	MCS1
21	MD6
22	MCS0
23	MD5
24	N/C
25	MD4
26	TDMA
27	MD3
28	OPT1
29	MD2
30	OPT0
31	MD1
32	MDACK
33	MD0
34	MDRQ
35	GND
36	+5

D7 D6 D5 D4 D3 D2 D1 D0
VCC
C12 100uF

LCD
LCD_D7
4

U1:E
11 10
74HC04

U1:F
13 12
74HC04

U16
DATA NC 6
NC 5
NC 4
NC 3
GND 1
2
DS2502-TSOC
NOT NORMALLY STUFFED

RP15 10k
VCC
8 7 6 5
1 2 3 4

J2
1 TCK 48
2 TDI 45
3 TDO 83
4 TMS 47
HEADER4X1

TCK
TDI
TDO
TMS

P1   J1
KPAD_Y1 ... KPAD_Y5
KPAD_X1 ... KPAD_X4
HEADER9X1
JMP 9X2 SHORT
KEYPAD ENCODER
UP TO 4X5 KEYS

TIE 6
TIE 58
TIE 59
TIE 65
TIE 66
TIE 70
TIE 71

NC 2
NC 19
NC 24
NC 34
NC 43
NC 46
NC 73
NC 80

TIE 72
TIE 76
TIE 78
TIE 79
TIE 81
TIE 82
TIE 86
TIE 93
TIE 94
TIE 96
TIE 99

VCCint 5
VCCint 57
VCCint 98
VCCio 26
VCCio 38
VCCio 51
VCCio 88

GND 69
GND 75
GND 84
GND 100
GND 21
GND 31
GND 44
GND 62

C5 100nF
C6 100nF
C7 100nF
C14 100nF
VCC

BD7 BD6 BD5 BD4 BD3 BD2 BD1 BD0

XC9500-SBX2

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Title SBX with LCD, KEYPAD, DIG I/O, & SERIAL I/O		
SBX INTERFACE		
Size B	Number	Rev 2
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A   B   C   D

4

U2
BD7 9 8D 8Q 12
BD6 8 7D 7Q 13
BD5 7 6D 6Q 14
BD4 6 5D 5Q 15
BD3 5 4D 4Q 16
BD2 4 3D 3Q 17
BD1 3 2D 2Q 18
BD0 2 1D 1Q 19
11 C
1 OC
74HC573 SOL20

U3
BD7 12 8Q 8D 9
BD6 13 7Q 7D 8
BD5 14 6Q 6D 7
BD4 15 5Q 5D 6
BD3 16 4Q 4D 5
BD2 17 3Q 3D 4
BD1 18 2Q 2D 3
BD0 19 1Q 1D 2
C 11
OC 1
74HC573 SOL20

READ REG ALWAYS CAPTURES
LAST WRITE OR READ DATA

SBX IF
LCD_DAT_WR

SERIAL I/O
DCE_DCD(L)
6

SBX IF
LCD_D7
3

VCC
C2 4.7uF

P3
16
15
14 LCD_D7
13 LCD_D6
12 LCD_D5
11 LCD_D4
10 LCD_D3
9 LCD_D2
8 LCD_D1
7 LCD_D0
6 LCD_EN
5 LCD_WR(L)
4 LCD_RS
3
VCC 2
100 NF C4 1
22-23-2161
LCD CONNECTOR 16X1

LCD W/O BACKLIGHT
CONSUMES 1.5 mA TYP @ 25C

SBX IF
LCD_DAT_RDOE(L)
LCD_DAT_RD
LCD_EN
LCD_WR(L)
LCD_RS

JP1
2 0
1 0
R1 10
R4 10

! DO NOT INSTALL JP1 IF
LCD MODULE DOES
NOT HAVE A CURRENT
LIMITING RESISTOR!

U4 DS1804
1 INC VCC 8
2 U/D H 3
7 CS W 5
4 GND L 6
{Value}

RP14 10k

U5
BD7 19 D8 Q8 17 LOCAL_LED(L)
BD6 18 D7 Q7 16 LCD_BL1
BD5 13 D6 Q6 15 LCD_CONT_CLK
BD4 12 D5 Q5 14 LCD_CONT_UP(H)
BD3 8 D4 Q4 7 LCD_BL0
BD2 3 D3 Q3 6 BUZ_DRV_L
BD1 2 D2 Q2 5 EXT_BUZ
BD0 1 D1 Q1 4 DCE_DCD(L)
MISCSTROBE 11 CLK
RST(L) 1 CLR RST(L)
TPIC6B273

LED1
GRN PG1111C
R5 470 VCC

BZ1
BUZZER

VCC

LCD CONTRAST,
BACKLIGHT, LED
& BUZZER

P4
2
1
VCC
PHOENIX2 100
EXTERNAL BUZZER OR LIGHT

BD[0..7]

VCC
C8 4.7uF
C9 100nF
C10 100nF
C13 100nF
C24 100nF

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LCD INTERFACE
Size B Number Rev 2
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WRITING A '1' TO THESE REGISTERS DRIVES THE CORRESPONDING OUTPUT LOW.

SBX IF

DOUT_WR2
DINP_RD2(L)
DOUT_WR1
DINP_RD1(L)
DOUT_WR0
RST(L)
DINP_RD0(L)
BD[0..7]
VCC

U8
BD7 19 D8 Q8 17 DIO_23
BD6 18 D7 Q7 16 DIO_22
BD5 13 D6 Q6 15 DIO_21
BD4 12 D5 Q5 14 DIO_20
BD3 9 D4 Q4 6 DIO_19
BD2 8 D3 Q3 5 DIO_18
BD1 3 D2 Q2 7 DIO_17
BD0 2 D1 Q1 4 DIO_16
11 CLK
1 CLR
TPIC6B273

U9
BD7 19 D8 Q8 17 DIO_15
BD6 18 D7 Q7 16 DIO_14
BD5 13 D6 Q6 15 DIO_13
BD4 12 D5 Q5 14 DIO_12
BD3 9 D4 Q4 6 DIO_11
BD2 8 D3 Q3 5 DIO_10
BD1 3 D2 Q2 7 DIO_9
BD0 2 D1 Q1 4 DIO_8
11 CLK
1 CLR
TPIC6B273

U10
BD7 19 D8 Q8 17 DIO_7
BD6 18 D7 Q7 16 DIO_6
BD5 13 D6 Q6 15 DIO_5
BD4 12 D5 Q5 14 DIO_4
BD3 9 D4 Q4 6 DIO_3
BD2 8 D3 Q3 5 DIO_2
BD1 3 D2 Q2 7 DIO_1
BD0 2 D1 Q1 4 DIO_0
11 CLK
1 CLR
TPIC6B273

U7
BD7 12 8Q 8D 9 DINP_R23
BD6 13 7Q 7D 8 DINP_R22
BD5 14 6Q 6D 7 DINP_R21
BD4 15 5Q 5D 6 DINP_R20
BD3 16 4Q 4D 5 DINP_R19
BD2 17 3Q 3D 4 DINP_R18
BD1 18 2Q 2D 3 DINP_R17
BD0 19 1Q 1D 2 DINP_R16
C 11
OC 1
74HC573 SOL20

U11
BD7 12 8Q 8D 9 DINP_R15
BD6 13 7Q 7D 8 DINP_R14
BD5 14 6Q 6D 7 DINP_R13
BD4 15 5Q 5D 6 DINP_R12
BD3 16 4Q 4D 5 DINP_R11
BD2 17 3Q 3D 4 DINP_R10
BD1 18 2Q 2D 3 DINP_R9
BD0 19 1Q 1D 2 DINP_R8
C 11
OC 1
74HC573 SOL20

U12
BD7 12 8Q 8D 9 DINP_R7
BD6 13 7Q 7D 8 DINP_R6
BD5 14 6Q 6D 7 DINP_R5
BD4 15 5Q 5D 6 DINP_R4
BD3 16 4Q 4D 5 DINP_R3
BD2 17 3Q 3D 4 DINP_R2
BD1 18 2Q 2D 3 DINP_R1
BD0 19 1Q 1D 2 DINP_R0
C 11
OC 1
74HC573 SOL20

RP2 10k
RP3 10k
10k RP5
10k RP4
VCC

RP6 10k
RP7 10k
10k RP8
10k RP9
VCC

RP10 10k
RP11 10k
10k RP13
10k RP12
VCC

DIO_23 DIO_22 DIO_21 DIO_20 DIO_19 DIO_18 DIO_17 DIO_16
DIO_15 DIO_14 DIO_13 DIO_12 DIO_11 DIO_10 DIO_9 DIO_8
DIO_7 DIO_6 DIO_5 DIO_4 DIO_3 DIO_2 DIO_1 DIO_0

UNDRIVEN INPUT BITS FLOAT HIGH, READ AS A '1'

OPTO-22 I/O RACK CONNECTOR STANDARD 25X2 RIBBON CABLE

24-CHANNEL: PIN 1 IS I/O
16-CHANNEL (AND LESS): PIN 1 IS VCC
(connecting DINP15 to VCC causes no harm, it just makes this input always read high)

THESE COMPONENTS ARE NOT NORMALLY STUFFED

I/O MODULES REQUIRE 15-150 mA EACH CONSULT MFGR DATA SHEETS. SEPARATE I/O RACK POWER MAY BE REQUIRED.
INSTALL JUMPER TO POWER I/O RACK FROM HOST SYSTEM

D1
CMSH2-40
JP2
C11 100uF
VCC

P8
PHOENIX2 100
VCC & GND

P5
IDC50M LPV LAT
DIO_23 DIO_22 DIO_21 DIO_20 DIO_19 DIO_18 DIO_17 DIO_16 DIO_15 DIO_14 DIO_13 DIO_12 DIO_11 DIO_10 DIO_9 DIO_8 DIO_7 DIO_6 DIO_5 DIO_4 DIO_3 DIO_2 DIO_1 DIO_0

C25 100nF C27 100nF C28 100nF C29 100nF C30 100nF C31 100nF
VCC

J7
HEADER 4X1
VCC

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SERIAL I/O

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ON BOTH ENDS OF BUS TRUNK
(TWO PLACES ONLY) ATTACH
120 OHM 1/2 W RESISTORS
DO NOT TERMINATE BUS STUBS!