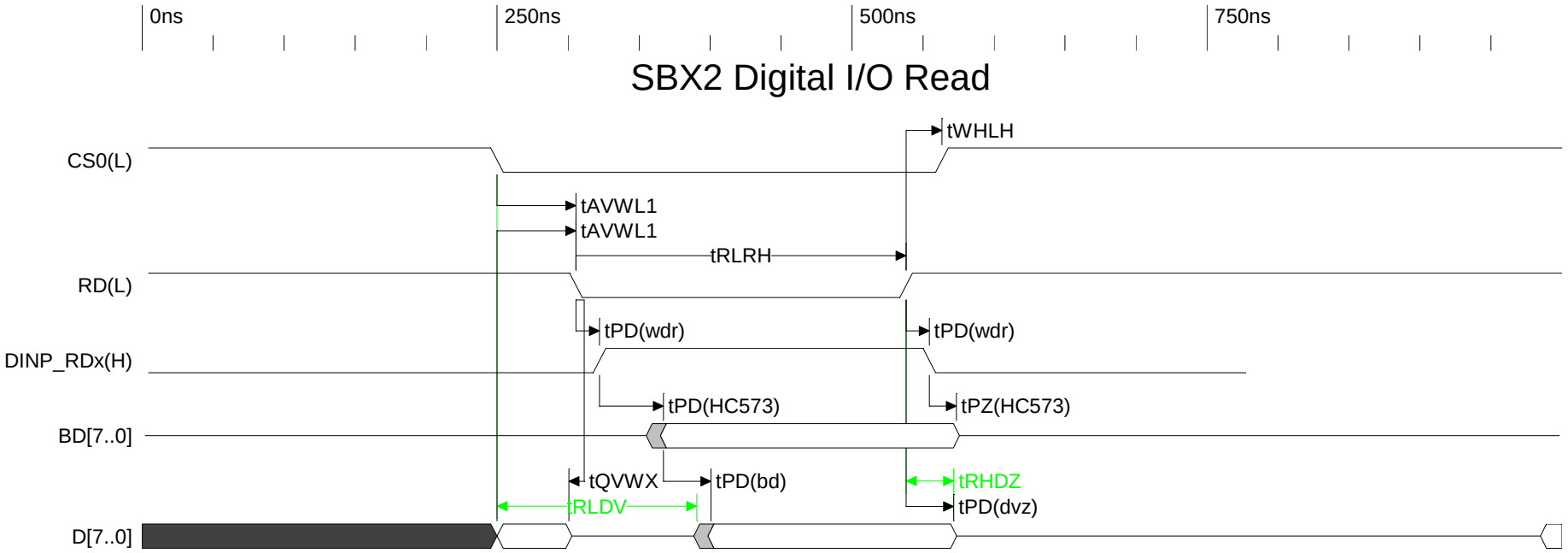

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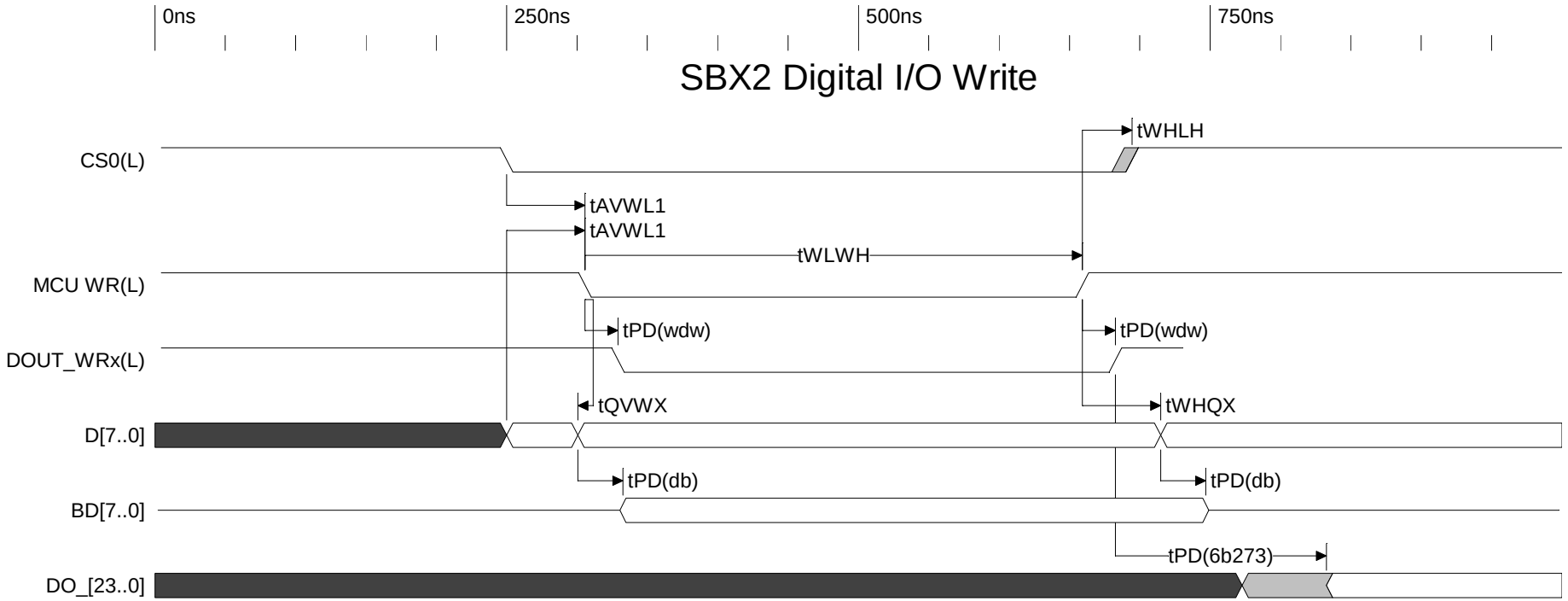
NOTES:
1. Signal names are from SBX2 Rev 3 schematics;
2. 33MHz uCAN2, 2 stretch cycles;

J:\PROJECTS\Sbx2\dev_hard\Sbx2_sch\Timing\SBX2_Digital_IO_Read.td

Row		Name	Formula	Min	Max	Margin	Comment
1	D	tPD(wdı	16.5	16.5	16.5		CPLD Delay RD(L) to DINP_RDx(L)
2	D	tPD(bd)	33.5	33.5	33.5		CPLD delay BUFDAT[7..0] to DAT[7..0]
3	D	tPD(dvz	33.5	33.5	33.5		CPLD delay RD(L) high to DAT[7..0] disabled
4	V	Cst	2	2	2		MCU MOVX Stretch cycles
5	V	tMCS	(4*tCLCL)	121.2	121.2		MCU clock multiplier
6	V	MCUclk	33	33	33		MCU crystal (in MHz)
7	V	tCLCL	(1000/MCUclk)	30.30	30.30		MCU clock period (nS)
8	D	tRLRH	((Cst*tMCS)-10)	232.4	232.4		MCU WR(L) Pulse Width
9	D	tQVWX	[(-5),]	-5			MCU Data Valid to WR(L)
10	D	tAVWL1	[((0.5*tMCS)-5),]	55.60			MCU Address to RD(L) or WR(L)
11	D	tWHLH	[((0.25*tMCS)-5),]	25.30			MCU Delay Write high to CS0(L) high
12	D	tPD(HC	[35,45]	35	45		HC573 Delay OE to Q
13	D	tPZ(HC	19	19	19		HC573 Delay output disable OE to Q
14	C	tRLDV	[,((Cst*tMCS)-20)]		222.4	<,71.818>	MCU RD low to Data valid
15	C	tRHDZ	[,((0.5*tMCS)-5)]		55.60	<,22.106>	MCU Data float after read



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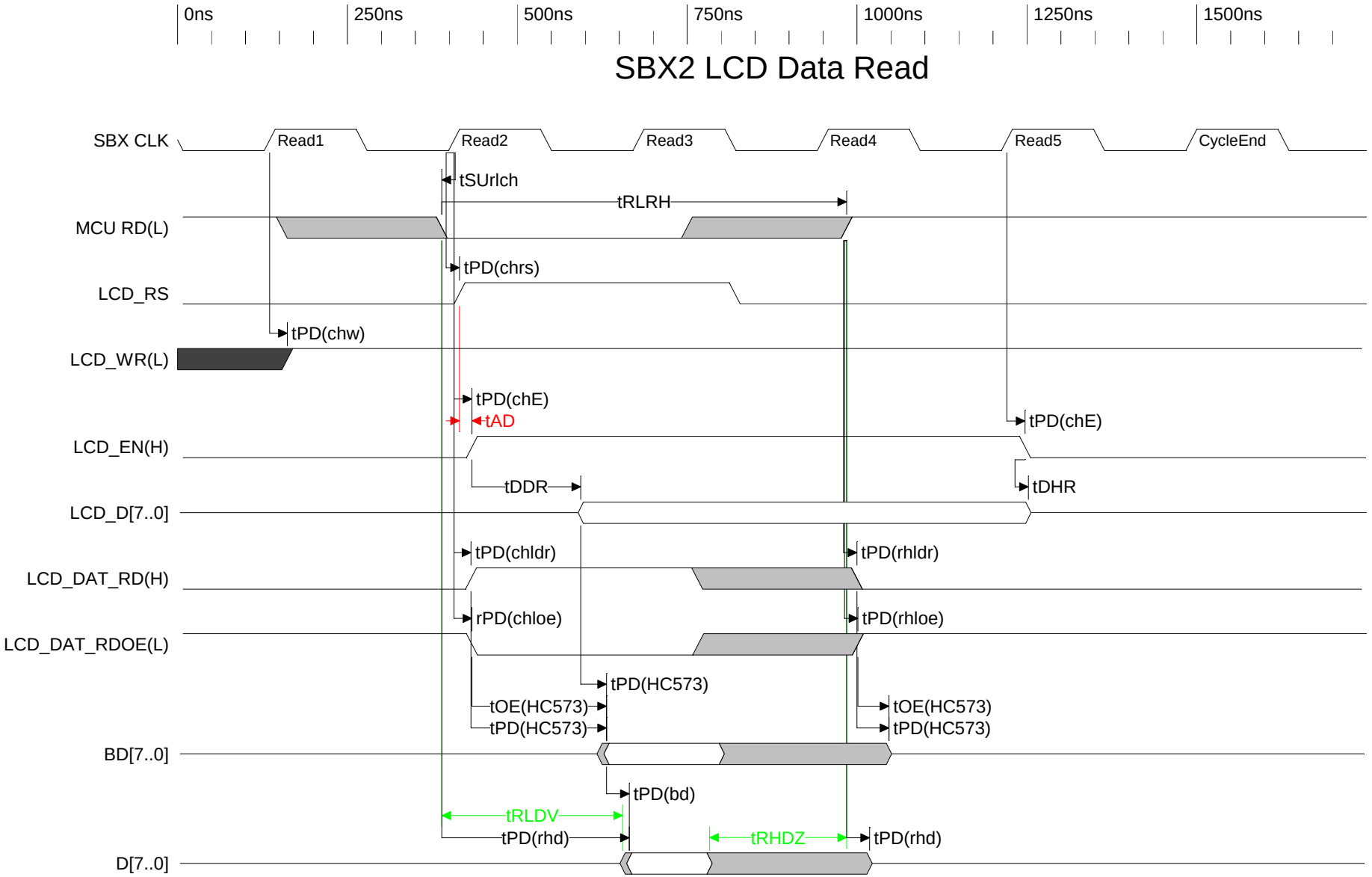
NOTES:
1. Signal names are from SBX2 Rev 3 schematics;
2. 33MHz uCAN2, 3 stretch cycles;

J:\PROJECTS\Sbx2\dev_hard\Sbx2_sch\Timing\SBX2_Digital_IO_Write.td

Row		Name	Formula	Min	Max	Margin	Comment
1	D	tPD(db)	32	32	32		CPLD delay DAT[7..0] to BUFDAT[7..0]
2	D	tPD(wd	23.5	23.5	23.5		CPLD Delay WR(L) to DOU_WRx(L)
3	V	Cst	3	3	3		MCU MOVX Stretch cycles
4	V	tMCS	(4*tCLCL)	121.2	121.2		MCU clock multiplier
5	V	MCUclk	33	33	33		MCU crystal (in MHz)
6	V	tCLCL	(1000/MCUclk)	30.30	30.30		MCU clock period (nS)
7	D	tWLWH	((Cst*tMCS)-10)	353.6	353.6		MCU WR(L) Pulse Width
8	D	tQVWX	[(-5),]	-5			MCU Data Valid to WR(L)
9	D	tAVWL1	[((0.5*tMCS)-5),]	55.60			MCU Address to RD(L) or WR(L)
10	D	tWHQX	[((0.5*tMCS)-5),]	55.60			MCU Data hold after write
11	D	tWHLH	[((0.25*tMCS)-5),((0.2	25.30	35.30		MCU Delay Write high to CS0(L) high
12	D	tPD(6b2	[90,150]	90	150		6b273 delay CLK to Q

SBX2 LCD Data Read



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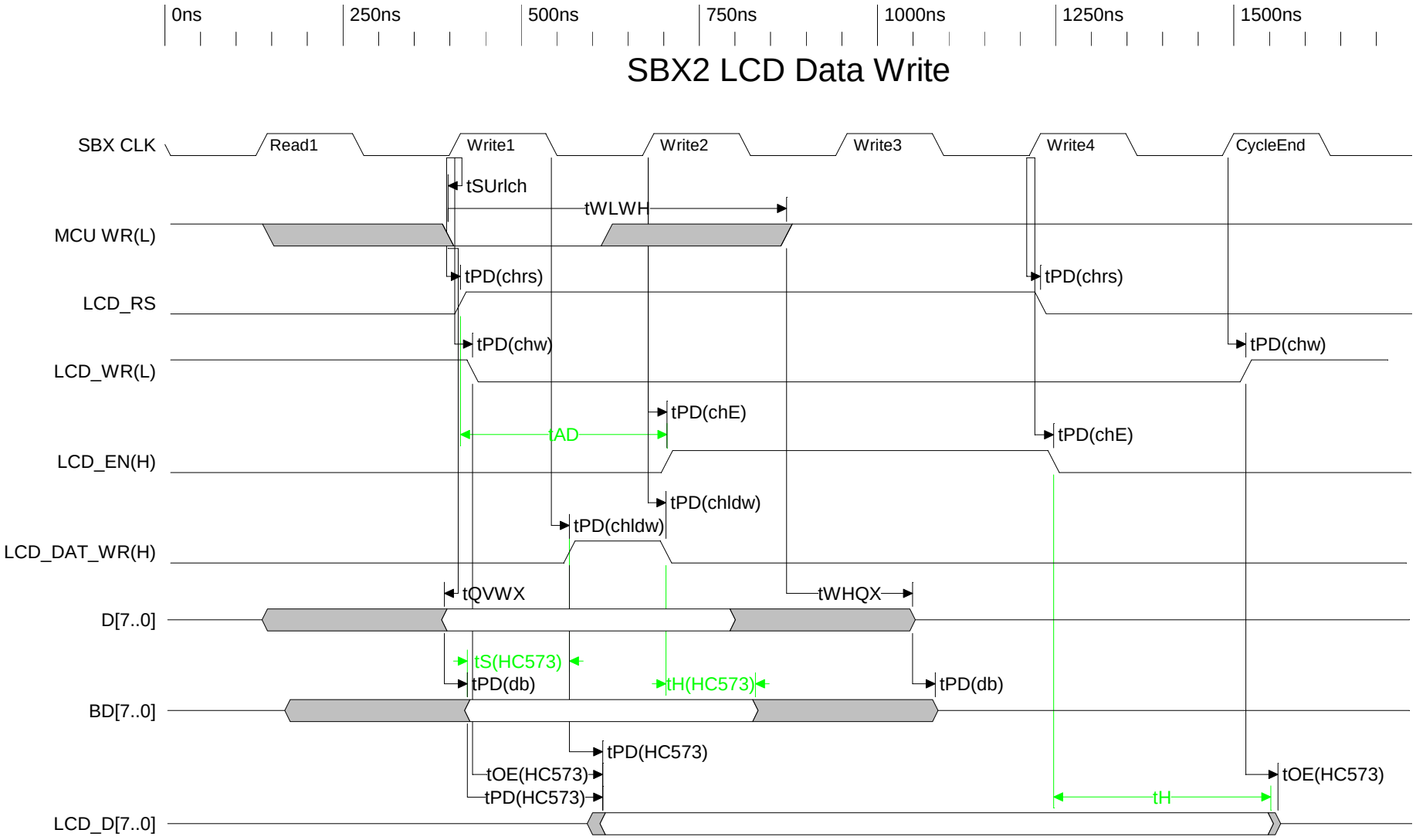
NOTES:
1. Instruction Read similar;
2. Signal names are from SBX2 Rev 3 schematics;
3. Sufficient stretch cycles overcomes the tAD violation.
4. 33MHz uCAN2 5 stretch cycles

J:\PROJECTS\Sbx2\dev_hard\Sbx2_sch\Timing\SBX2_LCD_Data_Read.td

Row		Name	Formula	Min	Max	Margin	Comment
1	V	SBXclk	3.686	3.686	3.686		SBX crystal (in MHz)
2	V	tSBX	(1000/SBXclk)	271.2	271.2		SBX clock period (nS)
3	D	tPD(chE	26.5	26.5	26.5		CPLD delay clock to LCD_EN
4	D	tPD(bd)	33.5	33.5	33.5		CPLD delay BUFDAT[7..0] to DAT[7..0]
5	D	tSUrlch	[(-(tSBX-18)),(-18)]	-253.2	-18		CPLD Setup time RD(L) before Clk high
6	D	tPD(chr	[,8]		8		CPLD Delay clock high to LCD_RS
7	D	tPD(chv	[,26]		26		CPLD Delay clock high to LCD_WR
8	D	tPD(rhlc	16.5	16.5	16.5		CPLD delay RD(L) to out
9	D	tPD(rhd	33.5	33.5	33.5		CPLD delay RD to DAT[7..0]
10	D	tPD(chl	25	25	25		CPLD delay clock high to LCD_DAT_RD
11	D	rPD(chl	26.5	26.5	26.5		CPLD clock high to LDS_DAT_RDOE
12	D	tPD(rhlc	15	15	15		CPLD delay RD high to LCD_DAT_RD
13	D	tPD(HC	[29,47]	29	47		HC573 delay LE to Q
14	D	tPD(HC	[28,38]	28	38		HC573 delay D to Q
15	D	tOE(HC	[35,45]	35	45		HC573 delay OE to Q
16	V	Cst	5	5	5		MCU MOVX Stretch cycles
17	V	tMCS	(4*tCLCL)	121.2	121.2		MCU Clock multiplier
18	V	MCUclk	33	33	33		MCU crystal (in MHz)
19	V	tCLCL	(1000/MCUclk)	30.30	30.30		MCU clock period (nS)
20	D	tRLRH	((Cst*tMCS)-10)	596.0	596.0		MCU RD(L) Pulse Width
21	C	tRHDZ	[,((1.5*tMCS)-5)]		176.8	<,143.318>	MCU Data float after read
22	D	tDDR	[,160]		160		LCD Module Data Delay Time (Read)
23	D	tDHR	[5,]	5			LCD Module Data Delay Time (Read)
24	C	tAD	[40,]	40		<-21.5,>	LCD Setup time address to E
25	C	tRLDV	[,((Cst*tMCS)-20)]		586.0	<,74.793>	MCU RD low to data valid



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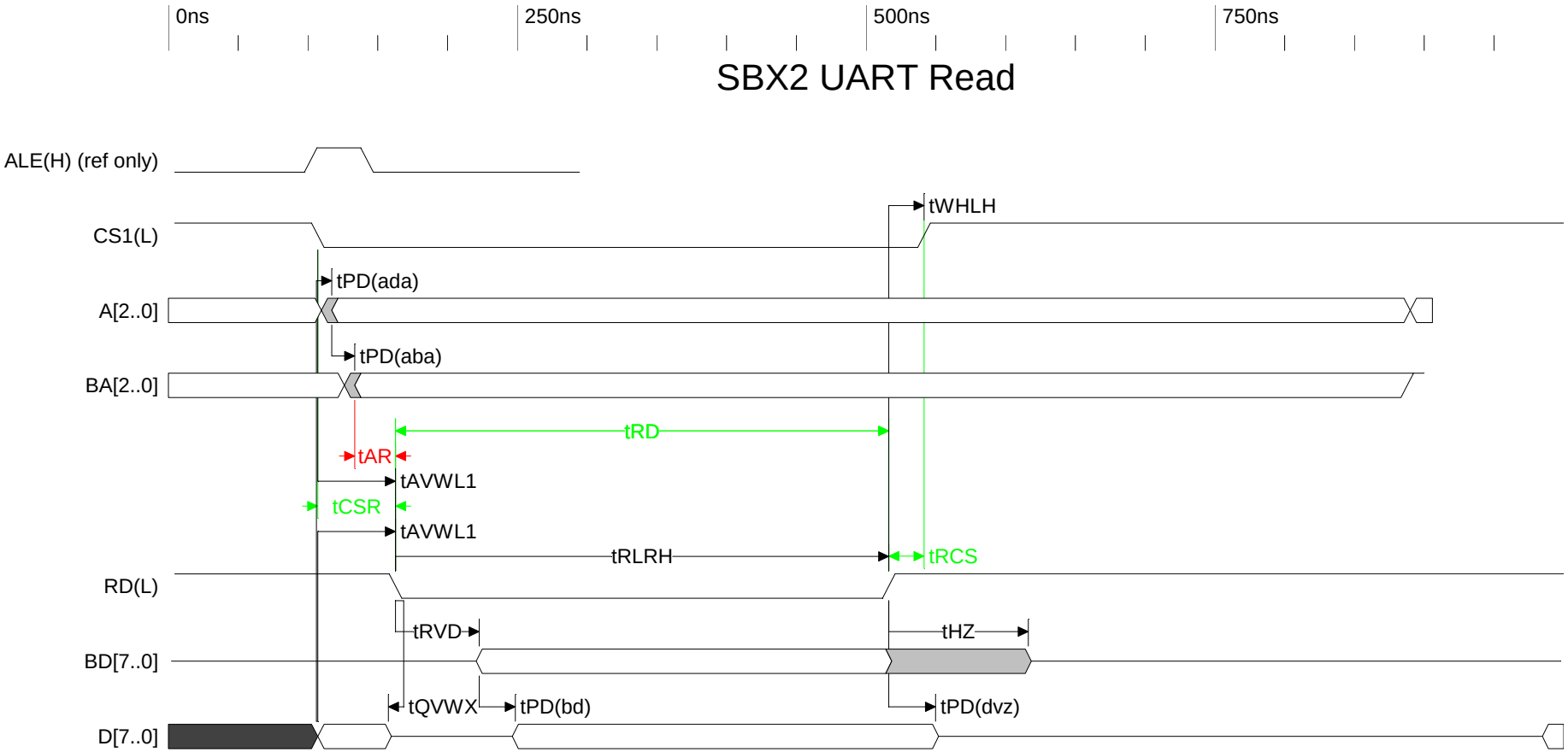
NOTES:
1. Instruction write similar;
2. Signal names are from SBX2 Rev 3 schematics;
3. 33Mhz uCAN2, 4 stretch cycles

J:\PROJECTS\Sbx2\dev_hard\Sbx2_sch\Timing\SBX2_LCD_Data_Write.td

Row		Name	Formula	Min	Max	Margin	Comment
1	V	SBXclk	3.686	3.686	3.686		SBX crystal (in MHz)
2	V	tSBX	(1000/SBXclk)	271.2	271.2		SBX clock period (nS)
3	D	tPD(chE	26.5	26.5	26.5		CPLD delay clock to E
4	D	tPD(db)	32	32	32		CPLD delay DAT[7..0] to BUFDAT[7..0]
5	D	tSUrlch	[(-(tSBX-9.5)),(-9.5)]	-261.7	-9.5		CPLD Setup time WR(L) before Clk high
6	D	tPD(chr	8	8	8		CPLD Delay clock high to LCD_RS
7	D	tPD(chv	25	25	25		CPLD Delay clock high to LCD_WR
8	D	tPD(chl	25	25	25		CPLD Delay clock to LCD_DATA_WR
9	V	Cst	4	4	4		MCU MOVX Stretch cycles
10	V	tMCS	(4*tCLCL)	121.2	121.2		MCU clock multiplier
11	V	MCUclk	33	33	33		MCU crystal (in MHz)
12	V	tCLCL	(1000/MCUclk)	30.30	30.30		MCU clock period (nS)
13	D	tWLWH	((Cst*tMCS)-10)	474.8	474.8		MCU WR(L) Pulse Width
14	D	tQVWX	[(-5),]	-5			MCU Data Valid to WR(L)
15	D	tWHQX	[((1.5*tMCS)-5),]	176.8			MCU Data hold after write high (Cst=0: [((0.25*tMCS)-5),]; Cst=1,2,3: [((0.5*tMCS)-5),];
16	D	tPD(HC	[28,38]	28	38		HC573 Delay D to Q
17	D	tPD(HC	[29,47]	29	47		HC573 Delay LE to Q
18	D	tOE(HC	[35,45]	35	45		HC573 Delay OE to Q
19	C	tS(HC5	[19,]	19		<124.134,>	HC573 Setup time data to LE
20	C	tH(HC5	[5,]	5		<120.632,>	HC573 Hold time LE to data
21	C	tH	[10,]	10		<294.767,>	LCD Data hold after E
22	C	tAD	[40,]	40		<249.767,>	LCD Setup time address to E

SBX2 UART Read



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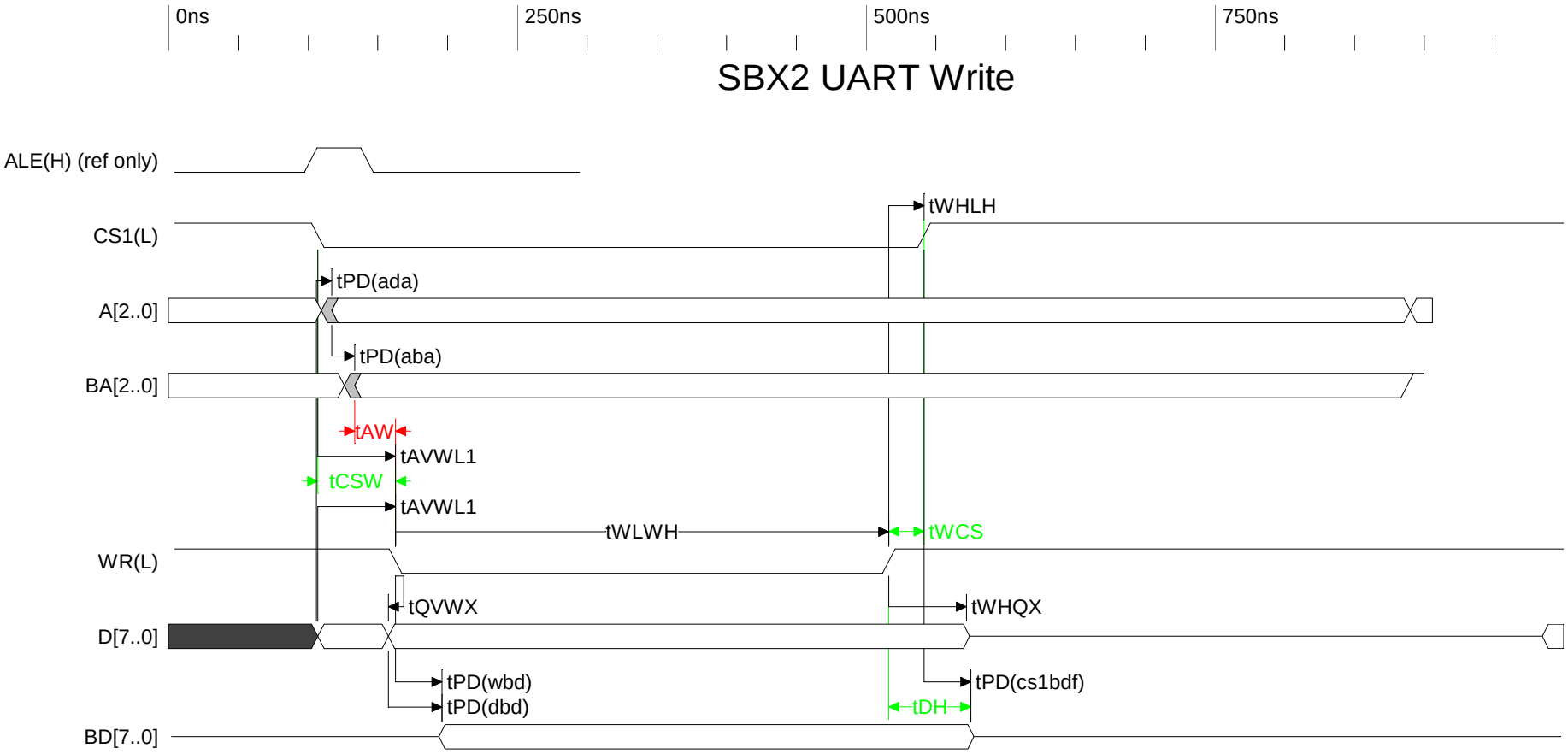
NOTES:
1. Signal names are from SBX2 Rev 3 schematics;
2. 33MHz uCAN2, 3 stretch cycles

J:\PROJECTS\Sbx2\dev_hard\Sbx2_sch\Timing\SBX2_UART_Read.td

Row		Name	Formula	Min	Max	Margin	Comment
1	D	tPD(bd)	26	26	26		CPLD delay BUFDAT[7..0] to DAT[7..0]
2	D	tPD(dvz	33.5	33.5	33.5		CPLD delay RD(L) high to DAT[7..0] disabled
3	D	tPD(aba	16.5	16.5	16.5		CPLD delay A[2..0] tp BA[2..0]
4	V	Cst	3	3	3		MCU MOVX Stretch cycles
5	V	tMCS	(4*tCLCL)	121.2	121.2		MCU clock multiplier
6	V	MCUclk	33	33	33		MCU crystal (in MHz)
7	V	tCLCL	(1000/MCUclk)	30.30	30.30		MCU clock period (nS)
8	D	tRLRH	((Cst*tMCS)-10)	353.6	353.6		MCU WR(L) Pulse Width
9	D	tQVWX	[(-5),]	-5			MCU Data Valid to WR(L)
10	D	tAVWL1	[((0.5*tMCS)-5),]	55.60			MCU Address to RD(L) or WR(L)
11	D	tWHLH	[((0.25*tMCS)-5),]	25.30			MCU Delay Write high to CS0(L) high
12	D	tPD(ada	[2.5,10]	2.5	10		MCU Delay AD[2..0] to A[2..0]
13	D	tLHLL	[((0.375*tMCS)-5),]	40.45			MCU ALE pulse width (for reference only)
14	D	tAVLL2	[(((-0.25)*tMCS)-5),]	-35.3(			MCU PCEx valid to ALE low (for reference only)
15	D	tRVD	[60,]	60			UART Delay RD to BD[7..0] active
16	D	tHZ	[0,100]	0	100		UART Delay RD to BD[7..0] floating
17	C	tAR	[30,]	30		<-0.894,>	UART RD delay from address
18	C	tCSR	[30,]	30		<25.606,>	UART RD delay from CS1
19	C	tRD	[125,]	125		<228.636,>	UART RD strobe width
20	C	tRCS	[20,]	20		<5.303,>	UART CS1 hold time from RD

SBX2 UART Write



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NOTES:
1. Signal names are from SBX2 Rev 3 schematics;
2. 33MHz uCAN2, 3 stretch cycles;

J:\PROJECTS\Sbx2\dev_hard\Sbx2_sch\Timing\SBX2_UART_Write.td

Row		Name	Formula	Min	Max	Margin	Comment
1	D	tPD(dbc	32	32	32		CPLD Delay D[7..0] to BD[7..0]
2	D	tPD(cs1	33.5	33.5	33.5		CPLD Delay CS1(L) to BD[7..0] floating
3	D	tPD(wb(	33.5	33.5	33.5		CPLD Delay WR(L) to BD[7..0] active
4	D	tPD(aba	16.5	16.5	16.5		CPLD delay A[2..0] tp BA[2..0]
5	V	Cst	3	3	3		MCU MOVX Stretch cycles
6	V	tMCS	(4*tCLCL)	121.2	121.2		MCU clock multiplier
7	V	MCUclk	33	33	33		MCU crystal (in MHz)
8	V	tCLCL	(1000/MCUclk)	30.30	30.30		MCU clock period (nS)
9	D	tWHQX	[((0.5*tMCS)-5),]	55.60			MCU Delay data hold after write high
10	D	tWLWH	((Cst*tMCS)-10)	353.6	353.6		MCU WR(L) Pulse Width
11	D	tQVWX	[(-5),]	-5			MCU Data Valid to WR(L)
12	D	tAVWL1	[((0.5*tMCS)-5),]	55.60			MCU Address to RD(L) or WR(L)
13	D	tWHLH	[((0.25*tMCS)-5),]	25.30			MCU Delay Write high to CS0(L) high
14	D	tPD(ada	[2.5,10]	2.5	10		MCU Delay AD[2..0] to A[2..0]
15	D	tLHLL	[((0.375*tMCS)-5),]	40.45			MCU ALE pulse width (for reference only)
16	D	tAVLL2	[(((-0.25)*tMCS)-5),]	-35.3(			MCU PCEx valid to ALE low (for reference only)
17	D	tLLAX2	[((0.125*tMCS)-5),]	10.15			MCU Address hold after ALE low (for reference only)
18	C	tAW	[30,]	30		<-0.894,>	UART RD delay from address
19	C	tCSW	[30,]	30		<25.606,>	UART RD delay from CS1
20	C	tWCS	[20,]	20		<5.303,>	UART CS1 hold time from WR
21	C	tDH	[30,]	30		<28.803,>	UART Data hold