SBX2 – REVISIONS

SCH REV	PCB REV	DATE	BY	DESCRIPTION	SCH REV	DATE	BY
0.0		00 June 20	wsk	Start of schematic capture based upon unreleased SBX1.			
1	1	00 July 25	wsk	Initial schematic capture complete.			
2	2	00 Aug 22	wsk	Sheet 3: Changed crystal oscillator load caps to 18pF; Added RP15; Sheet 4: Deleted LED1 & R2; Renamed LED2 to LED1; Changed LOCAL_LED(L) to DCE_DCD(L); Sheet 6: Added C20, P9, R13, R14, R15, RP16, RP17, U17; Changed P6 to 2mm header that supports the Systronix DTE / DCE / IrDA Dongle; Deleted R7 & R8; Connected U13 pin 24 to ground;			
3	3	01 Jul 03	wsk	Sheet 3: Disconnected UARTRD(L) & UARTWR(L) from U14; Routed RD(L) and WR(L) to sheet 6; Renamed J2 to P10; Added P11; Sheet 4: Added pullup RP14C to LCD_D7 to detect disconnected or unpowered LCD module; Sheet 6: Connected U6-21 & U6-25 to ground;			

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TO DO:

Silkscreen for standoff should be 6-32

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Title	SBX with LCD, KEYPAD, DIG I/O, & SERIAL I/O REVISIONS	
Size: B	Number:	Rev: 3
Date: Mon Aug 06, 2001		Drawn by: BAB/wsk
Filename: sbx2_030.sch		Sheet 1 of 6

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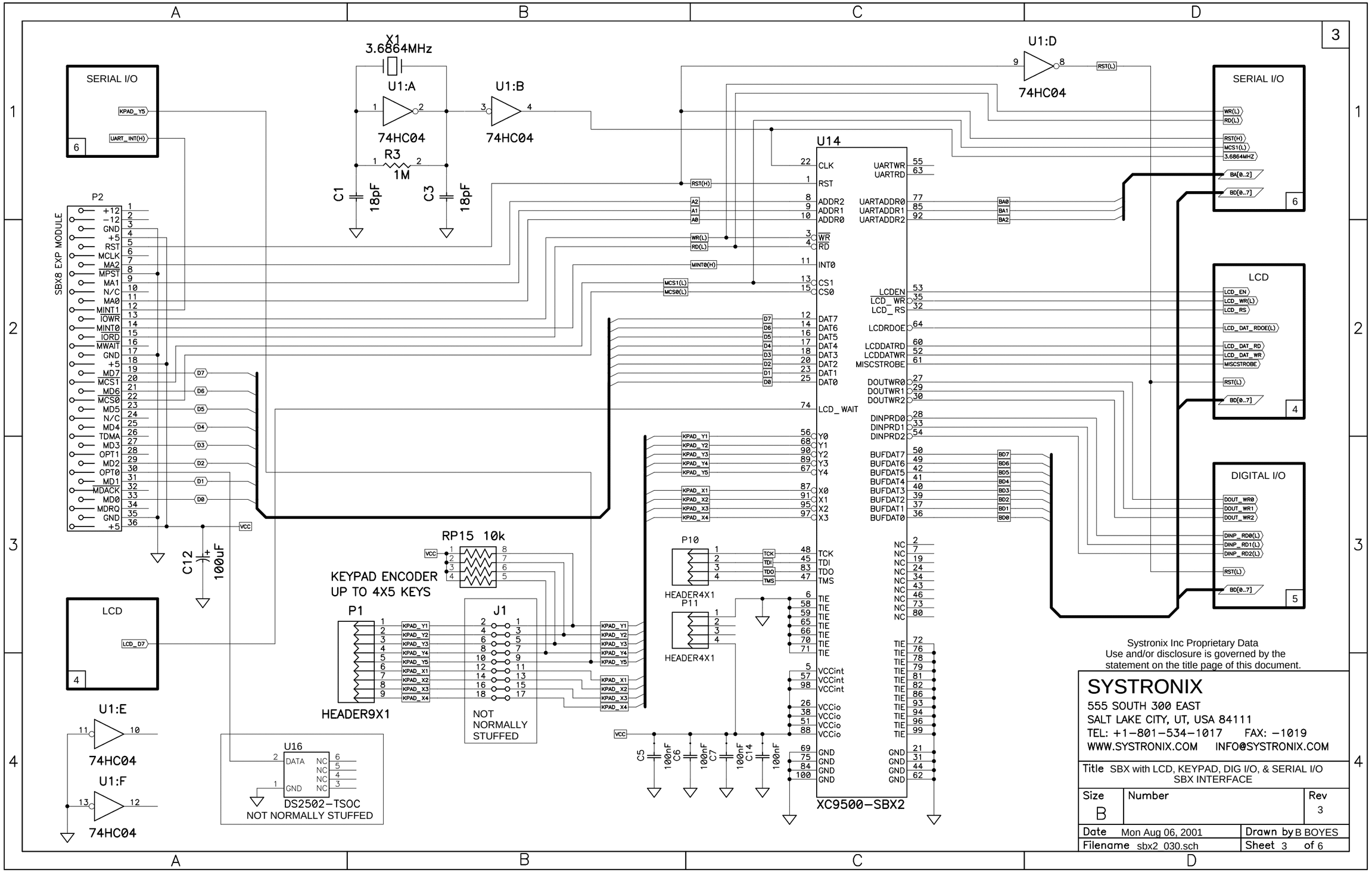
Title	SBX with LCD, KEYPAD, DIG I/O, & SERIAL I/O NOTES	
Size: B	Number:	Rev: 3
Date: Mon Aug 06, 2001		Drawn by: B BOYES
Filename: sbx2_030.sch		Sheet: 2 of 6


A
B
C
D
1
2
3
4
3
SERIAL I/O
KPAD_Y5
UART_INT(H)
6
X1
3.6864MHz
U1:A
74HC04
U1:B
74HC04
R3
1M
C1
18pF
C3
18pF
U1:D
74HC04
RST(L)
SERIAL I/O
WR(L)
RD(L)
RST(H)
MCS1(L)
3.6864MHZ
BA[0..2]
BD[0..7]
6
P2
SBX8 EXP MODULE
+12
-12
GND
+5
RST
MCLK
MA2
MPST
MA1
N/C
MA0
MINT1
IOWR
MINT0
IORD
MWAIT
GND
+5
MD7
MCS1
MD6
MCS0
MD5
N/C
MD4
TDMA
MD3
OPT1
MD2
OPT0
MD1
MDACK
MD0
MDRQ
GND
+5
D7
D6
D5
D4
D3
D2
D1
D0
VCC
C12
100uF
U14
CLK
RST
ADDR2
ADDR1
ADDR0
WR
RD
INT0
CS1
CS0
DAT7
DAT6
DAT5
DAT4
DAT3
DAT2
DAT1
DAT0
LCD_ WAIT
Y0
Y1
Y2
Y3
Y4
X0
X1
X2
X3
TCK
TDI
TDO
TMS
TIE
VCCint
VCCio
GND
UARTWR
UARTRD
UARTADDR0
UARTADDR1
UARTADDR2
LCDEN
LCD_ WR
LCD_ RS
LCDRDOE
LCDDATRD
LCDDATWR
MISCSTROBE
DOUTWR0
DOUTWR1
DOUTWR2
DINPRD0
DINPRD1
DINPRD2
BUFDAT7
BUFDAT6
BUFDAT5
BUFDAT4
BUFDAT3
BUFDAT2
BUFDAT1
BUFDAT0
NC
XC9500-SBX2
LCD
LCD_EN
LCD_WR(L)
LCD_RS
LCD_DAT_RDOE(L)
LCD_DAT_RD
LCD_DAT_WR
MISCSTROBE
RST(L)
BD[0..7]
4
DIGITAL I/O
DOUT_WR0
DOUT_WR1
DOUT_WR2
DINP_RD0(L)
DINP_RD1(L)
DINP_RD2(L)
RST(L)
BD[0..7]
5
RP15 10k
KEYPAD ENCODER
UP TO 4X5 KEYS
P1
HEADER9X1
J1
NOT
NORMALLY
STUFFED
P10
HEADER4X1
P11
HEADER4X1
C5
C6
C7
C14
100nF
LCD
LCD_D7
4
U1:E
74HC04
U1:F
74HC04
U16
DATA
GND
DS2502-TSOC
NOT NORMALLY STUFFED
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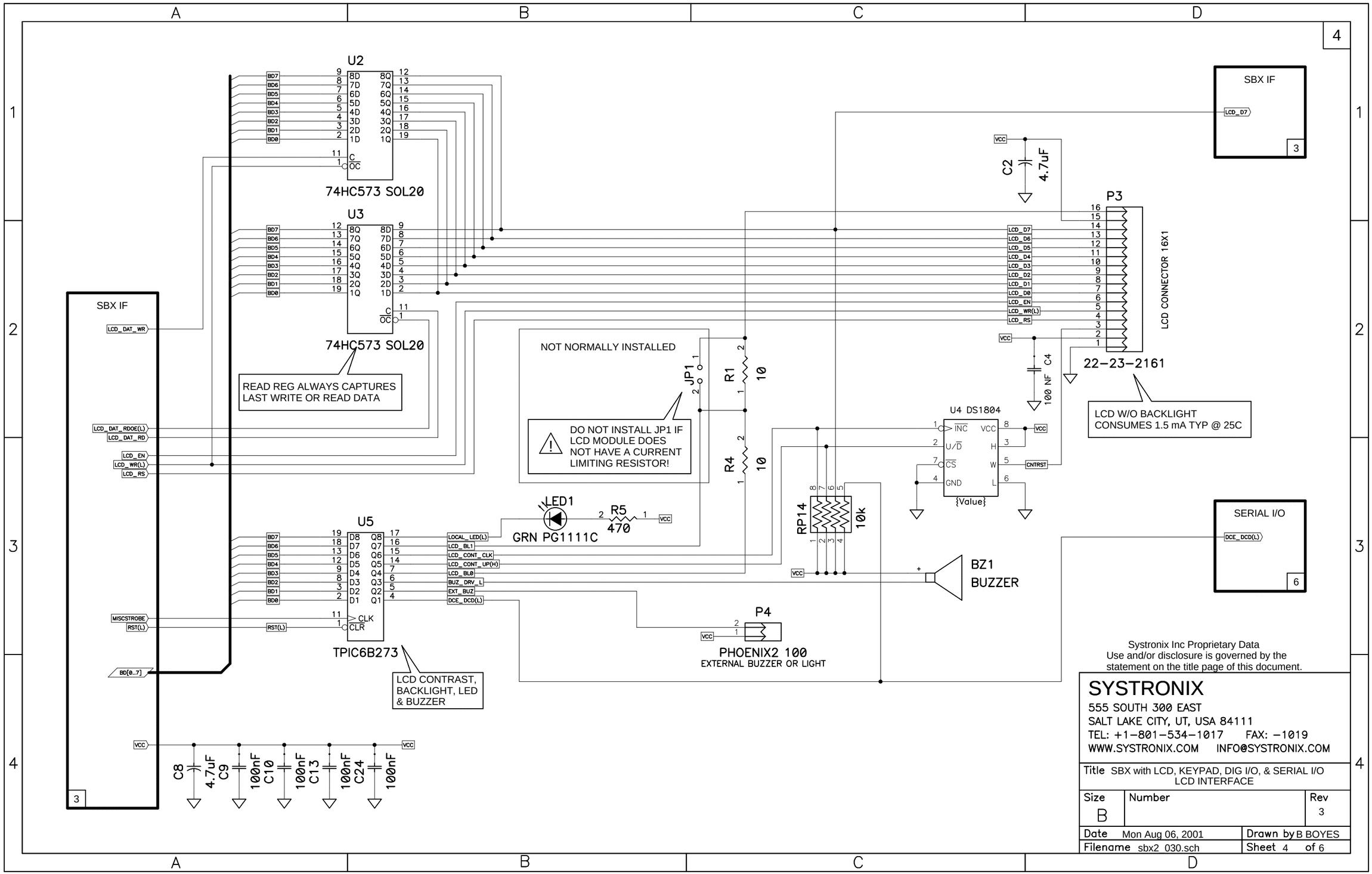
Title SBX with LCD, KEYPAD, DIG I/O, & SERIAL I/O
SBX INTERFACE
Size B
Number
Rev 3
Date Mon Aug 06, 2001
Drawn by B BOYES
Filename sbx2_030.sch
Sheet 3 of 6



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Size B	Number	Rev 3
Date Mon Aug 06, 2001		Drawn by B BOYES
Filename sbx2_030.sch		Sheet 4 of 6

WRITING A '1' TO THESE REGISTERS DRIVES THE CORRESPONDING OUTPUT LOW.

SBX IF

DOUT_WR2
DINP_RD2(L)
DOUT_WR1
DINP_RD1(L)
DOUT_WR0
RST(L)
DINP_RD0(L)
BD[0..7]

U8 TPIC6B273 — BD7..BD0 → DIO_23..DIO_16
U9 TPIC6B273 — BD7..BD0 → DIO_15..DIO_8
U10 TPIC6B273 — BD7..BD0 → DIO_7..DIO_0

U7 74HC573 SOL20 — BD7..BD0 → DINP_R23..DINP_R16
U11 74HC573 SOL20 — BD7..BD0 → DINP_R15..DINP_R8
U12 74HC573 SOL20 — BD7..BD0 → DINP_R7..DINP_R0

RP2 10k — DINP_R23..R20 → DIO_23..DIO_20
RP3 10k — DINP_R19..R16 → DIO_19..DIO_16
RP5 10k RP4 10k
RP6 10k — DINP_R15..R12 → DIO_15..DIO_12
RP7 10k — DINP_R11..R8 → DIO_11..DIO_8
RP8 10k RP9 10k
RP10 10k — DINP_R7..R4 → DIO_7..DIO_4
RP11 10k — DINP_R3..R0 → DIO_3..DIO_0
RP13 10k RP12 10k
VCC

UNDRIVEN INPUT BITS FLOAT HIGH, READ AS A '1'

C25 100nF C27 100nF C28 100nF C29 100nF C30 100nF C31 100nF

OPTO-22 I/O RACK CONNECTOR
STANDARD 25X2 RIBBON CABLE

24-CHANNEL: PIN 1 IS I/O
16-CHANNEL (AND LESS): PIN 1 IS VCC
(connecting DINP15 to VCC causes no harm, it just makes this input always read high)

P5 IDC50M LPV LAT — DIO_23..DIO_0

THESE COMPONENTS ARE NOT NORMALLY STUFFED

I/O MODULES REQUIRE 15-150 mA EACH CONSULT MFGR DATA SHEETS. SEPARATE I/O RACK POWER MAY BE REQUIRED.
INSTALL JUMPER TO POWER I/O RACK FROM HOST SYSTEM

D1 CMSH2-40
JP2
C11 100uF
P8 PHOENIX2 100 VCC & GND
J7 HEADER 4X1

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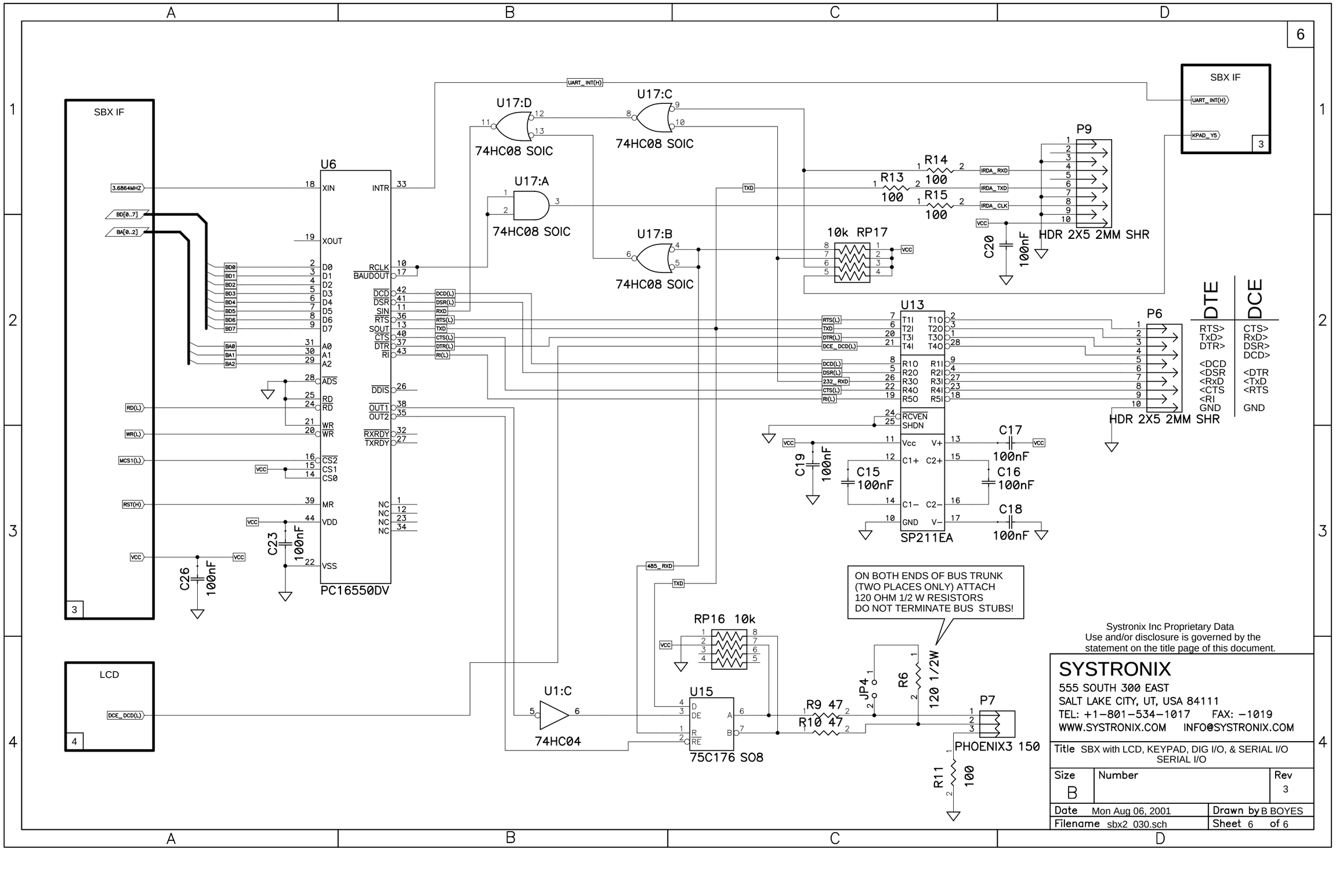

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